II. AMENDMENTS TO THE SPECIFICATION:

Please accept amendments to the specification as follows:

Page 1, after the title and before line 1, insert as a heading:

C1 BACKGROUND OF THE INVENTION

Page 1, between line 1 and the heading "BACKGROUND OF THE INVENTION", insert as a heading:

C2 1. Field of the Invention

Page 1, between line 14 and line 15, insert as a heading:

C3 2. Related Arts

Page 1, between line 25 and line 26, insert as a heading:

C4 SUMMARY OF THE INVENTION

Page 1, Fourth Paragraph (Lines 26 – 29), amended as follows:

C5 ~~Consequently, it~~ It is an object of the present invention to provide a method by means of which a LDMOSFET is obtained that is eminently suitable for the said application and, hence, functions perfectly at relatively high voltages and high frequencies. Besides, the method should be as simple and inexpensive as possible.

C6 Page 4, between line 24 and line 25, insert as a heading:

BRIEF DESCRIPTION OF THE DRAWINGS

Page 5, between line 2 and line 3, insert as a heading:

C7 DETAILED DESCRIPTION OF THE INVENTION

Page 5, Paragraph 1 (lines 3 – 26), amend as follows:

Figure 1 shows schematically and in a cross section perpendicular to the thickness direction a semiconductor device with a LDMOS transistor manufactured by means of a method according to the invention. The device comprises a semiconductor body 10 with a p-type silicon substrate 20 provided with a p-type epitaxial layer 21, having a thickness of 100 to 500 μm and 4 to 10 μm respectively and a resistivity of 5 to 1000 mΩcm and 5 to 30 Ωcm respectively. The LDMOSFET is surrounded by LOCOS (=Local Oxidation of Silicon) regions 22. Located on both sides of the n-type drain region 3, which has been provided with lowly doped part 3A, is the gate electrode 1 that is surrounded by n-type source region 2. In addition, the semiconductor body 10 contains a p-type plug region 23, which provides an electrical connection for the substrate 20 and a p-type channel region ~~24~~ 25 by means of which the conductivity properties of the LDMOSFET have been adjusted. The gate electrode 1, which is approximately 1 μm wide here, comprises a polycrystalline silicon layer 1 that is doped with P atoms and is positioned on a 50 to 90 nm thick gate oxide layer 4 of silicon dioxide, which extends over the surface of the semiconductor body 10 on both sides of the gate electrode 1. The latter is further provided with a lateral layer ~~25~~ 24 which contains silicon dioxide and against which spacers 5A of silicon nitride

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are positioned. Located on the upper side of the gate electrode 1 and in apertures 8, 9 in the gate oxide layer 4 situated over the source region 2 and the drain region 3, and in the present case in an isolating layer 26 covering the device, is a conductive layer 11 of titanium silicide. At the location of the gate electrode 1 and the part of the device located between the drain region 3 and the gate electrode 1, there is a shielding electrode 27 on the isolating layer 26. The part marked II of the device already contains the parts that are essential to the present invention, and the manufacture of the device by means of a method according to the invention will be discussed with reference to that part of figure 1.

Page 5, paragraph 2 (Page 5, line 27 to page 6, line 12), amend as follows:

Figures 2 to 9 show schematically and in a cross section perpendicular to the thickness direction the part of the semiconductor device marked II in Figure 1 in successive stages of the manufacture, using an exemplary embodiment of a method according to the invention. Taken as a basis (see figure 2) is a p-type silicon substrate 20 <u>(figure 1)</u> that is covered with a p-type epitaxial layer 21 <u>(figure 1)</u>. The surface of the semiconductor body 10 is then provided with a LOCOS region 22 <u>(figure 1)</u>, within which a gate oxide layer 4 is formed. Deposited on it is a 200 to 500 nm thick gate electrode 1 of polycrystalline silicon that is covered with a 5 to 10 nm thick intermediate layer 30 of silicon dioxide and a 100 to 300 nm thick shielding layer 31 of silicon nitride. Next, using the gate electrode 1 and a masking layer that is located on it and to the right thereof and is not shown in the figures, a p-type channel region 25 <u>(figure 1)</u> is formed by implantation of boron ions, in the present case at a flux of 2 to 8 times 10^{13} at/cm^2 and at an

energy of 30 to 90 keV. Then a 1 μm thick first additional masking layer 6 in the form of a photoresist layer 6 is deposited on and to the left of the gate electrode 1. After that, the n-type lowly doped part 3A of the drain region 3 (figure 1) is formed by implantation of P ions. In this example the flux and energy amount to 1 to 6 times 10^{12} at/cm^2 and 10 to 160 keV respectively. Next, after removal of the resist layer 6, the atoms of both the p-type channel region 25 (figure 1) and those of the lowly doped part 3A of the drain region 3 (figure 1) are electrically activated by a heat treatment at 950 to 1000°C for 20 to 60 minutes. In this process also the crystal damage caused by the implantations is repaired and the said regions 25 (figure 1), 3A diffuse up to the desired position under the gate electrode 1.

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